PLEASE AMEND THE SPECIFICATION AS INDICATED BELOW:

Page 6, paragraph [0032]:

Referring now to Fig. 2, according to the present invention, a circuit diagram for a ballast controller that incorporates power factor correction is illustrated generally as circuit 25. Circuit 25 has three MOSFET switches, M1,[[M1]] M2 and M3 for driving the various stages of the ballast control. Switches M1 and M2 comprise the half-bridge used to drive the ballast output and control the lamp power. Switch M3 controls the power factor correction for ballast control circuit 25. The PFC circuit operates in critical conduction mode to give a high power factor with a low total harmonic distortion. During each switching cycle, switch M3 is operated to turn on when the inductor current is discharged to zero, thereby obtaining rapid response and good DC bus regulation for the PFC circuit. Integrated circuit (IC) U1 is, for example, illustrated as a product of International Rectifier Corporation, the details of which are available in IR-2166 data sheet, the contents of which are hereby incorporated by reference in their entirety. IC U1 provides programmable control for the lamp ballast, and can be programmed to provide designated frequencies for preheat and normal operation. The preheat time can be programmed, in addition to dead time for circuit switching, over-current protection operation and end-of-life and fault protection. IC U1 also provides other protective features such as protection against failure of the lamp to strike, failure of a lamp filament, lamp end-of-life protection, DC bus under-voltage reset operation, as well as an automatic restart function.

Page 7, paragraph [0034]:

Referring now to Fig. 4, a state machine diagram is illustrated showing operation of the ballast control with a given fluorescent lamp. In a state 32, power is applied to IC U1, which can be wired into ballast control circuit 25 as illustrated in Fig. 2. Circuit 25 can also be provided on a ballast control card as described in U.S. Application No. 10/309,359, filed December 2, 2002. When power is applied to integrated circuit U1, the state machine illustrated in Fig. 4 moves to state 33, which

provides various initialization and start-up checks and operations. In state 33, an under-voltage lock-out mode is established when VCC is below the turn-on threshold of IC U1. In this mode, the output drivers for switches M1 and M2 are deactivated. When IC U1 is in UVLO mode, the circuit maintains a very low supply current, for example, less than 400 μA. The low supply current permits ICU1 to function and verify various circuit conditions before [[they]] operating the switches M1 and M2. In addition, state 33 shows the preheat time signal deactivated, and the oscillator is disabled. IC U1 leaves state 33 once VCC has reached the appropriate threshold, for example, 11.5 volts, and there are no lamp faults detected.